

Meg Freebern

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PROFILE

I love engineering – it’s how my brain works. I have worked in the DRAM industry eight years. I’m passionate about good design and want to work with sharp, creative people who give attention to detail and have excellent communication skills. I have a family and a few gigs on the side, so I am looking for something part time.

COMPUTER & DESIGN SKILLS

Digital circuit design
Layout analysis
Circuit analysis
Full-chip simulation
Verilog simulation

Cadence tools
Testbench creation
Root-cause identification
C++
PERL

RELEVANT EXPERIENCE

Qimonda, formerly Infineon, Williston, VT

Senior Engineer, DRAM Product Development

2003 – 2008

- Designed and tested low power, consumer DRAM and cellular pseudo-SRAMs.
- Developed block-level test benches to ensure first-time-right hardware.
- Specialized in SDR and DDR global control, SDR data path, column path, and full-chip verification.
- Implemented new features for emerging markets, resulting in twelve patent applications and, to date, three patents.

IBM, Essex Junction, VT

Engineer, Test Software Engineering

2002 – 2003

- Developed automation software to generate graphical bit-failure maps for RAMs, reducing turn-around time from weeks to minutes.

Engineer, DRAM Design

2000 – 2002

- Created methodologies to ensure comprehensive, accurate, and efficient full-chip simulations.
- Coordinated test strategy between design and test areas. Designed and verified test circuitry to improve troubleshooting techniques and device learning.

PATENTS

Parallel Datapath Architecture

US7245552B2

- Multiple, mask or fuse selectable data paths allow for a single chip design to fill wide market needs by operating at multiple data rates and over a wider range of speeds.

RAM Having Fast Column Access

US7082049B2

- Redesigned column address latching to reduce column access time, resulting in a higher performance product for the customer.

RAM Including Selective Activation of Select Line

US7248511B2

- Improved product reliability for the customer by reducing potential for bit failures due to new specification allowances and manufacturing variability.

EDUCATION

University of Vermont, Burlington, VT

Masters Courses in Electrical Engineering

- VLSI Digital Circuit Design and VHDL
- DRAM Architecture
- Business & Patent Law

Clarkson University, Potsdam, NY

Bachelor of Science, GPA 3.9

- Major in Computer Engineering, Concentration in Math

PROFESSIONAL DEVELOPMENT

Chittenden County Regional Planning Commission, VT

Town Representative, Appointed

2004 – Present

- Volunteer board member involved in writing policy and reviewing developments